

Design Verification Engineer

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Company: Apple

Location: Israel

Category: other-general

Summary:

In this visible role, you will be responsible for taking part of a SoC verification process of a large scale SoC. You will develop verification test plans, tools, test benches, protocol monitors, and high-coverage stimulus vectors. Apply advanced techniques to achieve verification with the highest quality, productivity, and time-to-market. You will work closely with the design team to ensure timely delivery of quality designs. Working with methods to accelerate verification time. Involvement in Post Silicon Validation. The position is relevant to all Apple sites: Herzliya, Haifa and Jerusalem

Key Qualifications:

+3 years experience in SoC Verification. You will need to have advanced knowledge of SoC architecture/design & in-depth knowledge of verification flow. Expected to have a deep understanding and shown experience in advanced verification process, including dynamic, coverage based and formal methods. Familiarity with verification environments, UVM, SystemVerilog – an advantage. Knowledge of formal, hardware acceleration – an advantage. Scripting and programming experience using several of the following: Perl, e, Verilog, SystemVerilog, C, C++, and TCL.

Description:

Imagine what you could do here. At Apple, new ideas have a way of becoming great products, services, and customer experiences very quickly. Bring passion and dedication to your job and there's no telling what you could accomplish. The people who work here have reinvented entire industries with all Apple Hardware products. The same passion for

innovation that goes into our products also applies to our practices - strengthening our dedication to leave the world better than we found it. Join us to help deliver the next groundbreaking Apple products.

Additional Requirements:

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