

DFT/Synthesis Design Engineer

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Company: SEQUANS

Location: Tel Aviv-Yafo

Category: other-general

PARIS OR SOPHIA ANTIPOLIS, FRANCE – TEL AVIV, ISRAEL – SINGAPORE

Responsible for writing timing constraints, running synthesis and implementing DFT (including scan, MBIST and IP testing), you will work on Sequans' next generation 5G IC and interact with software, signal processing algorithms, integration and layout teams.

REQUIRED EXPERIENCE

Engineering degree in a relevant discipline. BSc, MSc or equivalent

Minimum of 4 years experience of ASIC synthesis (including writing SDC), DFT (including scan and MBIST) and equivalence check, ideally with Cadence tools.

Knowledge of CPF and Cadence CLP is a bonus

PROFILE

Highly motivated, pro-active self-starter

Strong sense of ownership and responsibility

Creative thinker with strong problem solving skills

Team oriented attitude and ability to thrive in a multicultural environment

Excellent written and oral communications skills

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