IP Design Verification Engineer

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Company: Apple

Location: Israel

Category: other-general

Summary:

This role is for a Design Verification Engineer who will enable us to produce fully functional first silicon IP designs. The responsibilities include all phases of pre-silicon verification including but not limited to: establishing DV methodology, test-plan development, verification environment development including stimulus and checkers, test-writing, debug, coverage, sign-off for RTL freeze and tape-out.At Apple, we work every single day to craft products that enrich people's lives. Do you love working on challenges that no one has solved yet? Do you like changing the game? We have an opportunity for an exceptionally talented Design Verification Engineer. As a member of our dynamic group, you will have the rare and rewarding opportunity to craft upcoming products that will delight and encourage millions of Apple's customers every single day. The position is relevant to all Apple sites: Herzliya, Haifa and Jerusalem

Key Qualifications:

3+ years' experience in digital logic design verification.Basic knowledge of SystemVerilog and UVM.Experience developing UVM based IP test-benchesExperience with complex designs and advanced debug skills ability Experience with verification tools such as simulators, waveform viewers, build/run automation, coverage collection and analysis, gate level simulationsStrong communication skills are a must, as the candidate will interface with a lot of different groups within the company.Ability to work well in a team and be productive under tight schedules PREFERREDExcellent knowledge of one of the scripting languages: Python, Perl, TCLExperience with serial/parallel protocols such as PCIe or DRAMProven

knowledge of formal verification methodologyIn lieu of UVM knowledge, C/C++ experienced level knowledgeExperience with Lab hands-on debug

Description:

In this role, you will be responsible for ensuring bug-free first silicon for part of the IP and are expected to: Develop detailed test and coverage plans based on the micro-architecture Develop verification methodology suitable for the IP, ensuring a scalable and portable environment. Develop verification environment, including all the respective components such as stimulus, checkers, assertions, trackers, coverage and more.

Additional Requirements:

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