

Verification Engineer

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Company: Maof HR

Location: Tel Aviv-Yafo

Category: other-general

a global product company is looking for Senior Verification Engineer to join our growing verification group, to make a wide impact on the company's product.

In our team, you will find engaging, motivated, and energetic troubleshooters who work collaboratively with integrity and curiosity to make a difference. You can be yourself, do the work you love, and teach and learn from industry gurus all while being a vital part of this incredible journey.

Key Responsibilities

Plan, Design, and implement UVM based verification environments in block, fullchip and system levels

Verify the design and hunt for bugs, working closely with other teams

Build sophisticated, automated & randomized environments to cover all corners of the design

Use state of the art verification tools and technologies

Enhance the verification cycle time by building automation infrastructure

Required Qualifications

דרישות

5+ years of hands-on experience in functional verification

In-depth Knowledge in VLSI verification flow, languages & concepts

Experience in verification environments using SystemVerilog & UVM

Experience debugging RTL from block-level to system-level

Scripting knowledge – python, csh/bash, perl, TCL, etc.

Electronics Engineering degree

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